REMARKS

Applicant thanks the Examiner for her thoughtful review of the application. The status of the claims is as follows: **Claims 1 – 16** (Group I) are **Pending** and were elected for examination on the merits in response to a Restriction Requirement mailed on **27 September 2004**; and **Claims 17 – 22** (Group II) are **Withdrawn** from consideration as non-elected claims in the restriction requirement. New **Claims 23 – 26** were added in this response. Amendments to **Claims 1, 15,** and **17** are described below in the **PRESENT AMENDMENT**.

i. **PRESENT AMENDMENT**

Independent **Claim 1** as amended herein now recites that a read operation is non-destructive to a resistive state of the multi-resistive state element. Support can at least be found in Paragraph 0046 of the **Detailed Description.**

Dependent **Claim 15** was amended to further recite that the sidewall layer is operable as a dual-function etch stop layer and a diffusion layer. Support can at least be found in Paragraph 0055 of the **Detailed Description** and in **FIG. 11** of the **Drawings.**

Independent method **Claim 17** was amended to further recite that the multi-resistive state element layer is capable of being placed in at least two different states, each state exhibiting a different I-V curve, wherein a determination of state can be made non-destructively. Support can at least be found in Paragraphs 0046 – 0048 of the **Detailed Description.**

New independent **Claim 23** claims a conductive memory device including a multi-resistive state element having a bottom face with a fourth surface area that is less than a second surface area of a top electrode. Support can at least be found in **FIG. 11** of the **Drawings** (see reference numerals **815** and **810**).

New **Claims 24, 25,** and **26** depend from independent **Claim 23.** New **Claim 24** claims the first surface area is larger than the third surface area. New **Claim 25** claims the first surface area is not equal to the third surface area. Support can at least be found in **FIG. 11** of the **Drawings** (see reference numerals **810** and **805**). New **Claim 26** claims a read operation is non-destructive to a resistive state of the multi-resistive state element. Support can at least be found in Paragraph 0046 of the **Detailed Description.**

No new matter was introduced in amending the claims.

ii. ARGUMENT

a. Rejections of Claims 1 – 4, and 7 – 8 under 35 U.S.C. §102(b) and §102(e)

As amended herein, independent **Claim 1** is patentably distinct, is not anticipated by, and is non-obvious in view of the prior art cited in the Office Action mailed on **December 21, 2004**. Therefore, the rejection of **Claim 1** under **35 U.S.C. §102(b)** in view of U.S. Patent **6,249,014** to *Bailey* ought to now be withdrawn. Furthermore, all claims depending from **Claim 1** are patentably distinct, are not anticipated by, and are non-obvious in view of the prior art of record. Consequently, the rejection of **Claim 1** under **35 U.S.C. §102(b)** ought to now be withdrawn.

Specifically, *Bailey* does not explicitly or inherently disclose a conductive memory device that includes a multi-resistive state element where a read operation to the multi-resistive state element is non-destructive to a resistive state of the multi-resistive state element. Clearly, *Bailey* discloses in col. 1, lines 55 – 67 and col. 2, lines 1 – 6, that "*In either case, since a "read" to a ferroelectric memory is a destructive operation, the correct data is then restored to the cell during a precharge operation*" (emphasis ours).

For the same reasons as argued above for *Bailey*, the U.S. Patent **6,809,360** to *Kato* does not explicitly or inherently disclose a multi-resistive state element in which a read operation to the multi-resistive state element is non-destructive to a resistive state of the multi-resistive state element. It is well understood in the electronics art that a read operation to a capacitor based storage element of a ferroelectric random access memory (FeRAM) results in a destructive read of the data stored in the capacitor (e.g.

the PZT ferroelectric material) and a separate operation must be performed to restore the correct value of the data to the capacitor after the read operation. The semiconductor device of *Kato* is a FeRAM as is disclosed in col. 1, lines 19 – 39.

Therefore, as amended herein, **Claim 1** is not anticipated by, is patentably distinct, and is non-obvious in view of both *Bailey* and *Kato* and the rejection of **Claim 1** under **35 U.S.C. §102(b)** and **§102(e)** ought to now be withdrawn. Because **Claims 2 – 8** depend from **Claim 1** and inherit all of its limitations, those claims are not anticipated by, are patentably distinct, and are non-obvious in view of both *Bailey* and *Kato* and the rejection of those claims under **35 U.S.C. §102(b)** and **§102(e)** ought to now be withdrawn.

b. **Rejections of Claims 9 – 16 under 35 U.S.C. §103(a)**

As for **Claim 9**, a careful review of the cited sections of *Bailey* show that *Bailey* is silent as to forming a hard mask **830** over a top electrode **815** and the hard mask **830** has a surface area that is substantially similar to a second surface area of the top electrode **815** (see **FIGS. 9** and **10C – 10E** of the present application). In fact, a cursory glance at Figs. 2, 5, 7B, 8B, 9B, and 10B of *Bailey* clearly shows that the only connection to the top electrode is through the "local interconnect" that is used to electrically communicate the top electrode with other circuitry (see col. 7, lines 40 – 50). The local interconnect is not a hard mask layer that protects the top electrode of *Bailey* from subsequent etching processes and is therefore non-operative for that purpose. Moreover, an area of the local interconnect is not substantially similar to that of the top

electrode as is evident in the aforementioned figures. Instead, a small opening in the FEO layer 118 is opened and the local interconnect makes contact with the top electrode through the opening and only along a small portion of the surface area of the top electrode. Accordingly, *Bailey* is both silent and teaches away from the use of a hard mask having a surface area that substantially matches that of the top electrode it is in contact with and that serves as a barrier against subsequent etching steps.

Therefore, *Bailey* does not provide a road map to one or ordinary skill in the art, such that after reading *Bailey*, the hard mask of **Claim 9** would be an obvious addition to the structure of the memory device. Accordingly, **Claim 9** is not prima facie obvious in view of *Bailey* and the rejection of **Claim 9** under **35 U.S.C. §103(a)** ought to now be withdrawn.

As for **Claims 10 - 14**, *Bailey* is silent and teaches away from using a spacer **825** that surrounds only on the sides of the top electrode **815** as is clearly depicted in **FIGS. 9** and **10C – 10E** of the present application. Once again, a careful review of Figs. 2, 5, 7B, 8B, 9B, and 10B of *Bailey* clearly shows that the electrically insulating FEO **118**, the stress layers 884, 984, 1084, and 1184, cover both the side surfaces and a substantial portion of the top surface of the top electrode. *Bailey* does not suggest patterning and then etching those layers so that they cover only the sidewall surfaces of the top electrode. Therefore, there is no motivation for one skilled in the art upon reading *Bailey* to arrive at the spacer **825** of the present application. Accordingly, **Claims 10 - 14** are not prima facie obvious in view of *Bailey* and the rejection of those claims under **35 U.S.C. §103(a)** ought to now be withdrawn.

As for **Claim 15**, *Bailey* teaches away from an etch stop/diffusion barrier **820** that forms a sidewall layer that at least partially surrounds the side surfaces of the bottom electrode **805**, the multi-resistive state element **810** and the top electrode **815**. In contrast, *Bailey* teaches that his hydrogen barrier encapsulation technique serves to reduce or eliminate hydrogen induced degradation of ferroelectric capacitors by *completely encapsulating the capacitor* within a suitable hydrogen barrier material 1174 (see *Bailey* col. 13, lines 1 – 29 and Fig. 10b). The sidewall layer **820** of **Claim 15** does not completely surround the bottom electrode **805**, the multi-resistive state element **810** and the top electrode **815** as is clearly shown in **FIG. 11** and as disclosed in Paragraph 0055 of the **Detailed Description** of the present application.

Bailey does not provide a motivation to cover only the sidewalls of his ferroelectric capacitor because the objective of the hydrogen barrier 1174 is to completely encapsulate the capacitor to prevent the hydrogen degradation. Therefore, one skilled in the art upon a reading of *Bailey* would not be motivated to cover only the sidewall surfaces for the purpose of forming an etch stop/diffusion barrier **820** as claimed in **Claim 15**. Consequently, **Claim 15** is not prima facie obvious in view of *Bailey* and the rejection of **Claim 15** under **35 U.S.C. §103(a)** ought to now be withdrawn.

As for **Claim 16**, *Bailey* is silent as to any current flow or a leakage current flow that is parallel to a Z-axis. *Bailey* makes no mention whatsoever to X, Y, and Z axes, to current flow, or to leakage current flow. Moreover, the ferroelectric memory cell of *Bailey* senses data stored in the ferroelectric layer using charge and not current. If charge were allowed to flow out of the ferroelectric layer (i.e. a current), then the charge

would be depleted by the current flow and the data stored therein would be lost. Accordingly, one skilled in the art would not read *Bailey* and arrive at the Z-axis current flow of **Claim 16**. Consequently, **Claim 16** is not prima facie obvious in view of *Bailey* and the rejection of **Claim 16** under **35 U.S.C. §103(a)** ought to now be withdrawn.

iii. CONCLUSION

Applicant now believes the present application to be in condition for allowance, and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application the undersigned can be reached at (408) 737-7200 x124.

Respectfully submitted,
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